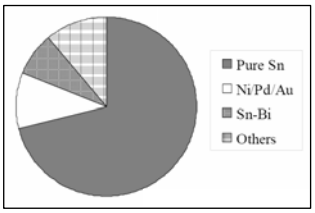
The Tin Myth: How the Hi-Rel Industry Won

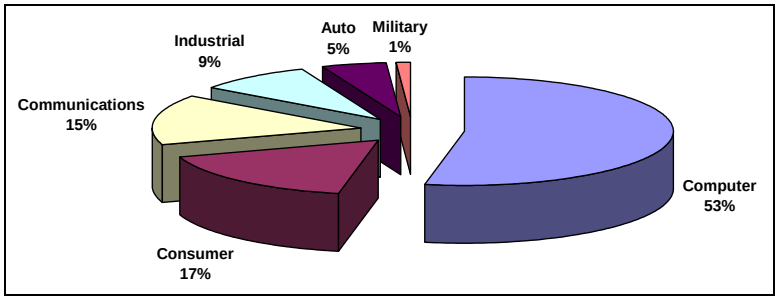
One of the greatest concerns during this transition to Pb-free electronics, and therefore Pb-free components, has been the supposed rapid and widespread adoption of pure tin plating as the solderability plating of choice. A number of questionable surveys have driven this belief, with some promoting that 'pure' tin has captured 75% or more of the market.



The response to this wave of tin-whisker susceptible components has been impressive. Numerous organizations have sprung up to either analyze (iNEMI, E4), inform (ELFNET, GEIA), or fight (NASA Tin Whisker Group) this potential reliability threat. Millions have been spent on testing, analysis, report writing, and, most importantly, material identification (have you bought stock in XRF companies?).

Why all this time, money, and effort? Because, supposedly, the electronics supply chain is backwards. Suppliers call the shots and the OEMs, especially those in Hi-Rel (telecom, industrial, military, avionics, medical, etc.), have no control over what goes in their product and out to the customer. Could we be more wrong?

While the military/avionics crowd has frequently focused on their ever shrinking portion of the pie, and their subsequent loss of influence, they have failed to realize that they have some pretty heavy allies in the fight over tin plating. Telecom, where tin plating is banned as per GR-78-CORE, industrial controls, and automotive are also very concerned about the use of tin plating. And these Hi-Rel industries combined comprise over 30% of the semiconductor marketplace. How's that for leverage? And this doesn't include high-end servers, which is often lumped in with all computers.



And don't forget the price markups for low-volume purchases. While Dell or Nokia might get the best price because they are buying in the millions, component manufacturers can make a significant portion of their profit from selling in lower volumes to OEMs and distributors.

What does all this mean? The Hi-Rel industry has much more leverage then it lends itself credit. And the component industry has responded. Two significant trends were recently identified based on a survey performed by DfR Solutions of the 50 leading semiconductor manufacturers.

At one level, component manufacturers have started to differentiate between fine-pitch and coarse-pitch components. This is a trend not picked up by the earlier surveys. As a general statement, fine-pitch is defined as 0.65 mm pitch or less and is primarily limited to thin scale outline packages (TSOP), thin scale small outline packages (TSSOP) and plastic quad flat packs (PQFP).

Within the fine-pitch family, the overwhelming majority of component manufacturers have selected either palladium platings (which don't whisker), tin-bismuth platings (which don't seem to whisker), or still offer SnPb platings for those so inclined. As seen in the table below, among the top 16 component manufacturers, only three do not offer whisker-resistant platings in their fine-pitch packaging: Intel, Freescale, and Micron. The decision by Freescale and Micron to go pure tin is especially mind-boggling, given their obvious efforts to market to the high-rel market (industrial controls, avionics, military).

Company	Package	Plating
Intel	QFP / TSOP	Sn[1]
Samsung	QFP / TSOP	NiPdAu
Texas Instruments	QFP / TSOP	NiPdAu
Toshiba	TSOP (Discretes)	NiPdAu
	TSOP (Memory)	SnAg or SnCu
	TSOP (LSI)	NiPdAu or SnAg or SnBi
STMicroelectronics	QFP / TSOP	NiPdAu[2]
Infineon	QFP	Sn or SnPb
	TSOP	NiPdAu
Renesas Technology	QFP	Mostly Sn-Cu, Sn-Bi; some NiPdAu[3]
	TSOP	Mostly NiPdAu, with some Sn-Cu, Sn-Bi[4]
Sony	QFP / TSOP	Pd or SnPb
Philips/NXP	QFP	Sn
	TSOP	NiPdAu
Hynix	TSOP	SnBi
Freescale	QFP / TSOP	Sn[5]
NEC	QFP / TSOP	Sn, SnBi, or NiPdAu
Micron	TSOP	Sn
Matsushita/Panasonic	QFP	Pd
	TSOP	SnBi
AMD	QFP	Sn, SnCu, or SnPb
IBM	QFP	N/A[6]
Qualcomm	N/A	N/A[7]
Fujitsu	QFP	SnBi
	TSOP	SnBi
Sharp	QFP	SnBi, NiPdAu[8]
	TSOP	SnBi

[1] Assumed. Unable to document
[2] The NiPdAu technology will be used for most of Signal SMD packages: SO, TSSOP, L/TQFP with few exceptions such as SMD packages with soft solder die attach, PLCC (due to the particular shape of the leads), TSOP (alloy 42), few L/TQFP, Exposed pad packages.
[3]
[4]
[5] 1 hour bake at 150C
[6] Offers very limited QFP options in ASIC format. Plating selected by customer
[7] No leaded devices identified in Qualcomm products (all area array)
[8] QFN devices will contain NiPdAu

Where do we go from here? The answer seems obvious. Rather than throwing their hands and leaving the reliability of their products to fate (or to expensive and questionable techniques such as solder dipping), the Hi-Rel industry should get together and do what OEMs do best: apply financial pressures to those hold outs who continue to insist on using tin plating.

Avionic/military (Honeywell, Rockwell Collins, Raytheon, Boeing, EADS, Thales), telecommunication (Lucent-Alcatel, Nortel, Cisco, Huawei, Siemens), industrial control (Honeywell, Emerson, Siemens), medical (Medtronic, Guidant, St. Jude Medical, Biotronik) and high-end server (EMC, Sun Microsystems, Dell, HP, IBM) companies should release a joint statement making it clear that pure tin plating on fine pitch components is unacceptable. With so few component manufacturers fabricating this risky configuration, the changeover to palladium or tin-bismuth[9] should be quick and painless.

The upside to this approach? The eventual elimination of expensive XRF equipment, research projects of questionable value, and a return to focusing on product and technology innovation. The exact same place we were ten years ago.

[9] Yes, there is the risk of a low-temperature SnPbBi alloy when soldering SnBi-plated components to SnPb solder. However, standard SnBi platings currently have 2-5 wt% bismuth to retard whisker growth. And, as stated by GEIA, this Bi content should be too low to form the low melt temperature Sn-Bi-Pb eutectic (96 °C melting point). There is a ternary Sn-Pb-Bi peritectic that is viable for Bi above 6% by weight in the component finish and this peritectic has a melting point of 135°C. As long as the Bi concentration on the lead is less than 6%, the peritectic should not be an issue [70].

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